WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

an antifuse including a first terminal, a second terminal and a gate dielectric between the first terminal and the second terminal, the first terminal being connected to a line;

a program driver circuit coupled to the second terminal of the antifuse; and

a bypass circuit coupled to the line and the program driver circuit, the bypass circuit being adapted to shunt current around the antifuse during a programming mode.

2. The integrated circuit of claim 1, wherein the bypass circuit includes a plurality diodes.

3. The integrated circuit of claim 2, wherein the plurality of diodes includes a plurality of transistors coupled together as series-connected diodes.

4. The integrated circuit of claim 3, wherein the plurality of transistors include p-channel transistors.

5. The integrated circuit of claim 1, wherein the gate dielectric includes at least one of an oxide and an oxynitride.

6. An integrated circuit, comprising:

a line to provide a programming voltage during a programming mode and to provide a common voltage during a non-programming mode;

an antifuse including a first terminal connected to the line, a second terminal and a gate dielectric between the first terminal and the second terminal;

a program driver circuit coupled to the second terminal of the antifuse; and

a bypass circuit coupled to the line and the program driver circuit in parallel with the antifuse, the bypass circuit being adapted to shunt current around the antifuse during the programming mode with the antifuse not being selected to be blown.

7. The integrated circuit of claim 6, wherein the line is a common bus line.

8. The integrated circuit of claim 7, wherein the line is adapted to connect to a high programming voltage during the programming mode.

9. The integrated circuit of claim 8, wherein the line is adapted to connect to an external pin to provide the high programming voltage.

10. The integrated circuit of claim 8, wherein the line supplies a voltage of approximately 7-8 volts during the programming mode.

11. The integrated circuit of claim 7, wherein the line is adapted to connect to an integrated circuit supply voltage during the non-programming mode.

12. The integrated circuit of claim 11, wherein the integrated circuit supply voltage is within a range of approximately one to five volts.

13. An integrated circuit, comprising:

an antifuse including a first terminal, a second terminal and a gate dielectric between the first terminal and the second terminal and including a silicide, the first terminal being connected to a line;

a program driver circuit coupled to the second terminal of the antifuse; and

a bypass circuit coupled to the line and the program driver circuit, the bypass circuit being adapted to shunt current around the antifuse during a programming mode.

14. The integrated circuit of claim 13, wherein the silicide of the gate dielectric consists essentially of tungsten silicide layer.

15. The integrated circuit of claim 14, wherein the gate dielectric includes a polysilicon layer.

16. The integrated circuit of claim 13, wherein the silicide of the gate dielectric consists essentially of titianium silicide.

17. The integrated circuit of claim 16, wherein the gate dielectric includes a polysilicon layer.

18. The integrated circuit of claim 13, wherein the silicide of the gate dielectric consists essentially of cobalt silicide.

19. The integrated circuit of claim 18, wherein the gate dielectric includes a polysilicon layer.

20. An integrated circuit, comprising:

an antifuse including a first terminal, a second terminal and a gate dielectric between the first terminal and the second terminal, the first terminal being connected to a line;

a program driver circuit coupled to the second terminal of the antifuse;

a gate bias circuit connected to the program driver circuit; and

a bypass circuit coupled to the line and the program driver circuit, the bypass circuit being adapted to shunt current around the antifuse during a programming mode.

21. The integrated circuit of claim 20, wherein the gate bias circuit is connected to the line.

22. The integrated circuit of claim 21, wherein the line is a common bus line that is connected to a high programming voltage during the programming mode and connected to an integrated circuit supply voltage during a non-programming mode.

23. The integrated circuit of claim 20, wherein gate bias circuit includes a high voltage transistor.

24. The integrated circuit of claim 23, wherein the high voltage transistor includes a gate comprising tungsten silicide, and wherein the first terminal comprises tungsten silicide.

25. The integrated circuit of claim 23, wherein the high voltage transistor includes a gate comprising titanium silicide, and wherein the first terminal comprises titanium silicide.

26. The integrated circuit of claim 23, wherein the high voltage transistor includes a gate comprising cobalt silicide, and wherein the first terminal comprises cobalt silicide.

27. The integrated circuit of claim 23, wherein the high voltage transistor includes a drain connected to the line.

28. An integrated circuit, comprising:

an antifuse including a first terminal, a second terminal and a gate dielectric between the first terminal and the second terminal, the first terminal being connected to a line;

a program driver circuit coupled to the second terminal of the antifuse;

a bypass circuit coupled to the line and the program driver circuit, the bypass circuit being adapted to shunt current around the antifuse during a programming mode; and

wherein the program driver circuit includes a first transistor, second transistor and third transistor connected in series.

29. The integrated circuit of claim 28, wherein the first transistor includes a drain connected to the second terminal, a gate connected to gate bias circuit, and a source connected to the second transistor.

30. The integrated circuit of claim 28, wherein the second transistor includes a first source/drain connected to the first transistor, a gate connected to an integrated circuit supply voltage, and a second source/drain connected to the third transistor.

31. The integrated circuit of claim 28, wherein the third transistor includes a first source/drain connected to the second transistor, a gate connected to a logic circuit providing a select signal to operate the third transistor, and a second source/drain connected to the ground voltage.

32. The integrated circuit of claim 28, wherein the second transistor and the third transistor are connected together in a cascode configuration.